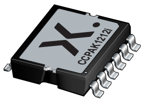


BUK7T1R4-100L

N-channel 100V, 1.35mΩ, Standard Level MOSFET in CCPAK1212i

26 August 2025 Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 12 low ohmic split-gate technology, for ultra-low $R_{DS(on)}$ capability, housed in a CCPAK1212i (SOT8005A) package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

Fully automotive qualified to AEC-Q101:

- 175 °C rating suitable for thermally demanding automotive environments.

Trench 12 split-gate trench technology:

- Reduced cell pitch enables enhanced power density resulting in lower conduction losses.
- Fast and efficient switching with optimal damping for low spiking and improved switching efficiency.

CCPAK mounting base

- Large cross-sectional area of exposed drain tab for excellent thermal dissipation and low steady state thermal resistance.

CCPAK gull-wing leads:

- High Board Level Reliability (BLR), pins absorbing mechanical stress during thermal cycling.
- Visual (AOI) soldering inspection, no need for expensive x-ray equipment.

CCPAK copper clip technology:

- Low transient thermal resistance and package inductance.
- High maximum current capability and improved current spreading on silicon die.

3. Applications

- Light-electric / Electric vehicle applications
- 48V to 12V DC-DC Converters
- Synchronous rectifier for On-Board Charging (OBC) systems
- 48V Traction Inverters
- 48V Belt Starter Generator (BSG)
- Battery Management Systems

4. Quick reference data

Table 1. Quick reference data

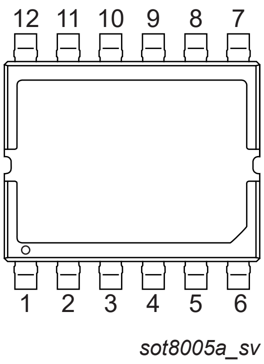
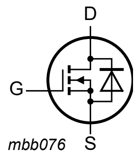
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	355	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	935	W
T_j	junction temperature			-55	-	175	°C

nexperia

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 9		-	1.07	1.35	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 10		-	2.4	3.1	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 11; Fig. 12		14	46	106	nC
$Q_{G(tot)}$	total gate charge	I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	228	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 CCPAK1212i (SOT8005A)	
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	G	gate		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7T1R4-100L	CCPAK1212i	Plastic, surface mounted copper clip package (CCPAK1212i); 12 terminals; 2.0 mm pitch, 12 mm × 12 mm × 2.5 mm body	SOT8005A

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7T1R4-100L	X7T1R410L

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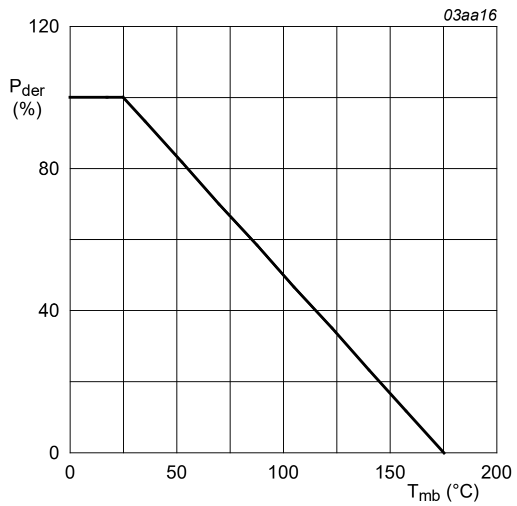
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

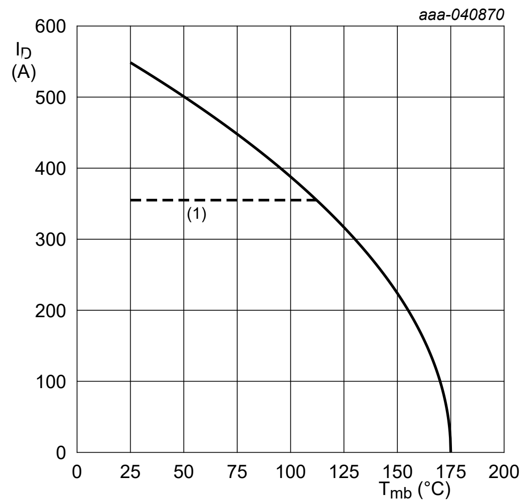
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	935	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	355	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	355	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	2195	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	355	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	2195	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 99 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 175 µs; Fig. 4	[1]	-	1130	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[1]	-	99	A

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

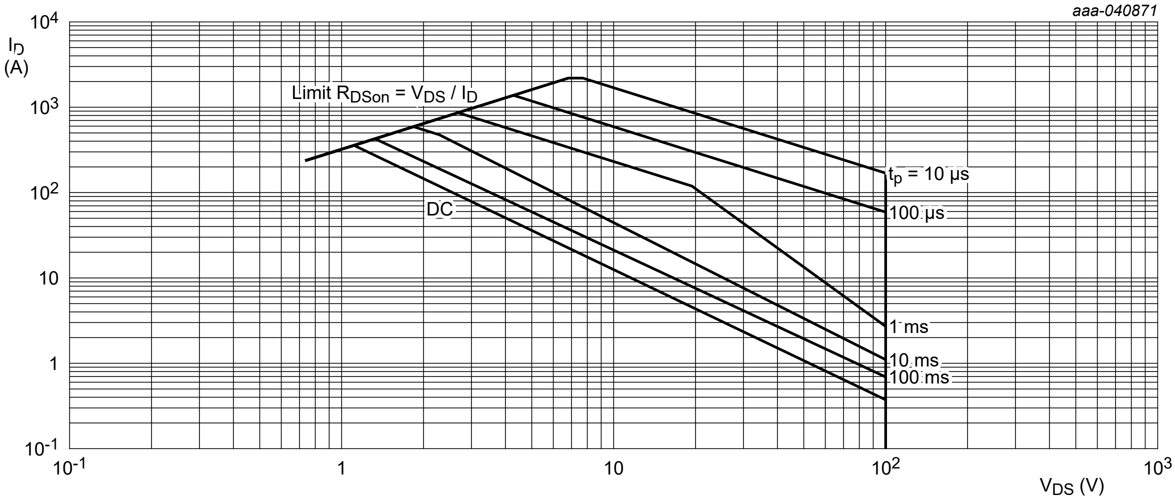
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 10 V

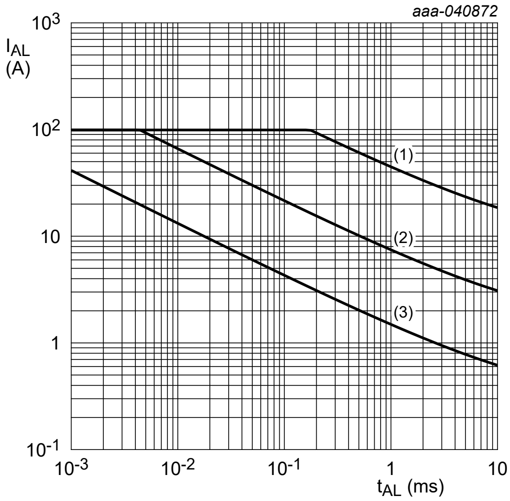
(1) 355 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\,(init)}$ = 25 °C; (2) $T_{j\,(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.123	0.16	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	30	-	K/W
		With exposed pad contacting a fixed temperature heatsink. Thermal interface material is 50 µm thick and has 0.5W/mK thermal conductivity.	[1]	-	1.2	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.

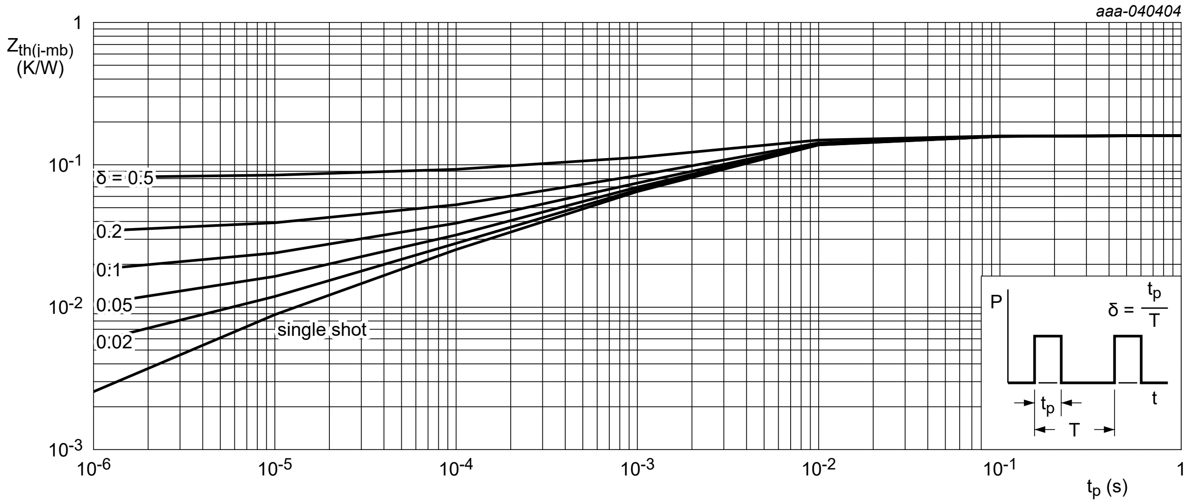


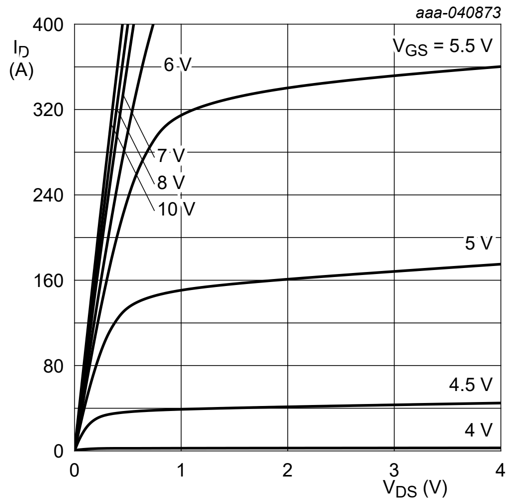
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

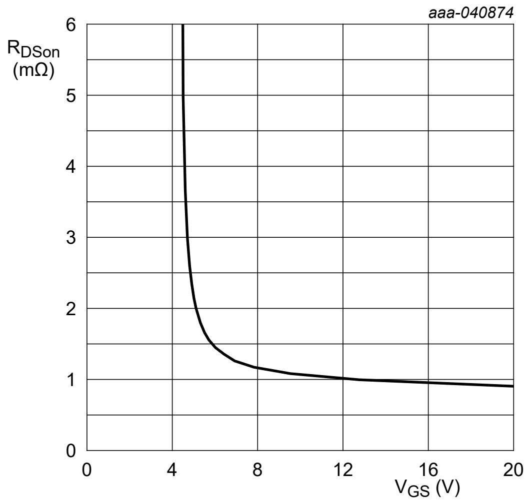
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2	3.1	4	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	1.61	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3.7	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-9.4	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.05	1.6	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	35	160	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 9		-	1.07	1.35	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 10		-	1.7	2.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 10		-	2.4	3.1	mΩ
		V_{GS} = 7 V; I_D = 25 A; T_j = 25 °C; Fig. 9		-	1.36	2.04	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.51	1.02	2.05	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 11; Fig. 12		128	255	383	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	228	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 11; Fig. 12		46	76.5	107	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	51	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	25.4	-	nC
Q_{GD}	gate-drain charge			14	46	106	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 50 V; T_j = 25 °C; Fig. 11; Fig. 12		-	4.4	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 13		10901	18168	25436	pF
C_{oss}	output capacitance			2494	4157	6652	pF
C_{rss}	reverse transfer capacitance			9	92	239	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	67	-	ns
t_r	rise time			-	63	-	ns
$t_{d(off)}$	turn-off delay time			-	157	-	ns
t_f	fall time			-	84	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 14		-	0.76	1	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 15		-	62	-	ns
Q_r	recovered charge			-	74	-	nC



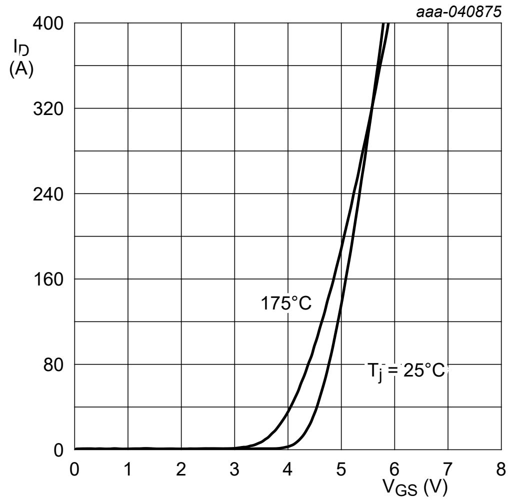
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



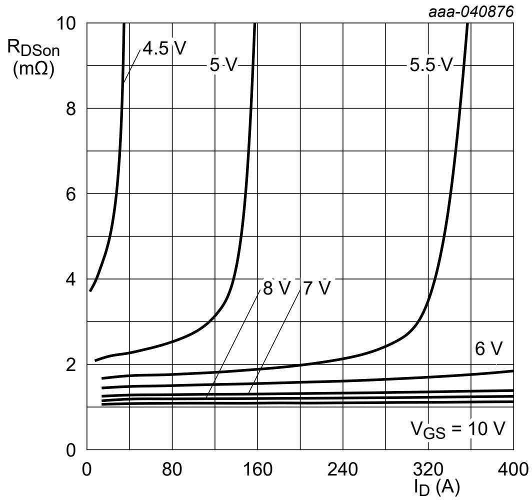
T_j = 25 °C; I_D = 25 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



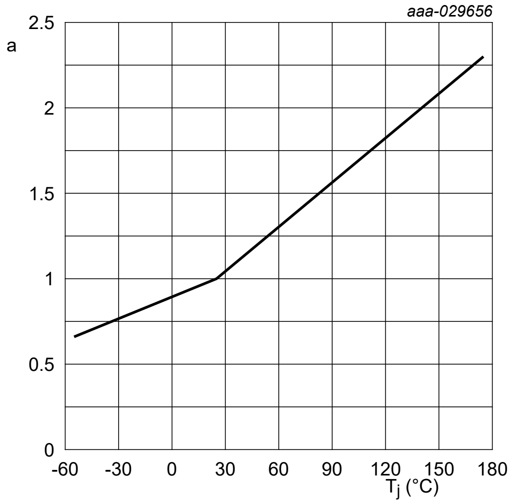
V_{DS} = 8 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



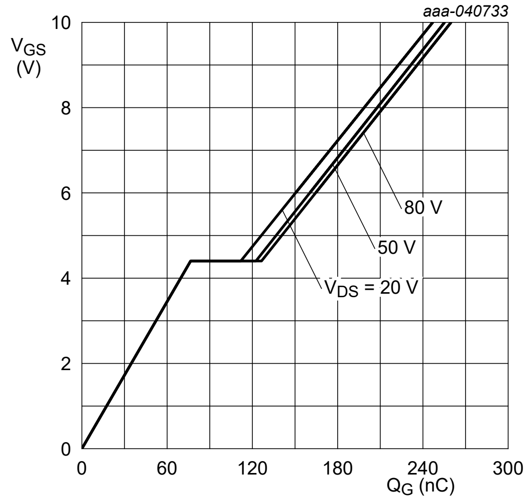
T_j = 25 °C

Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 11. Gate-source voltage as a function of gate charge; typical values

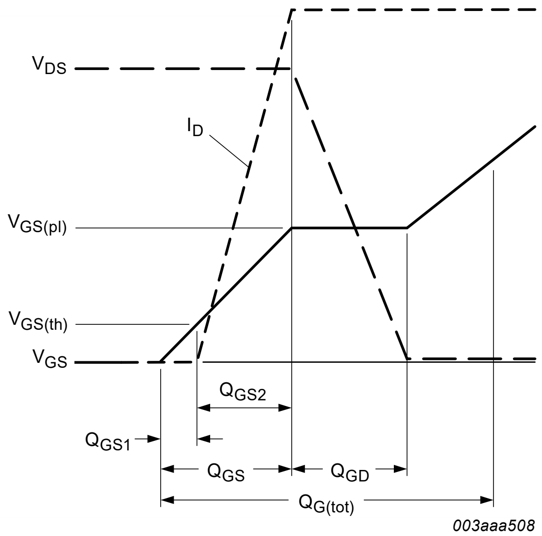
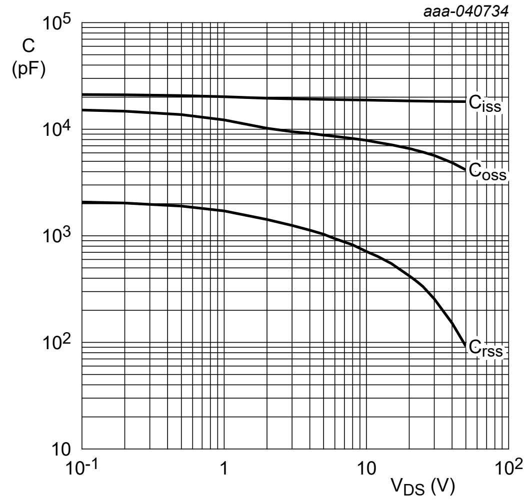


Fig. 12. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

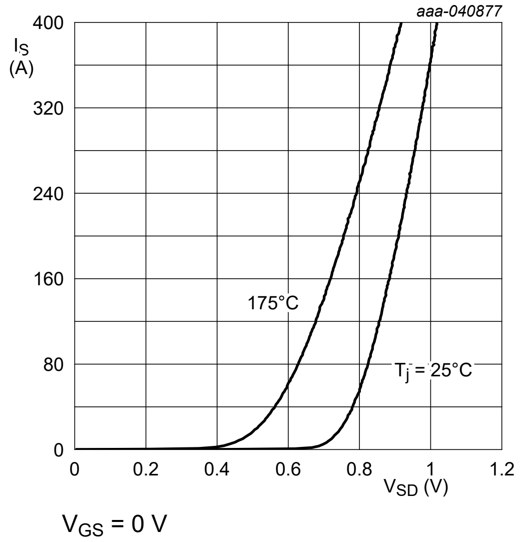


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

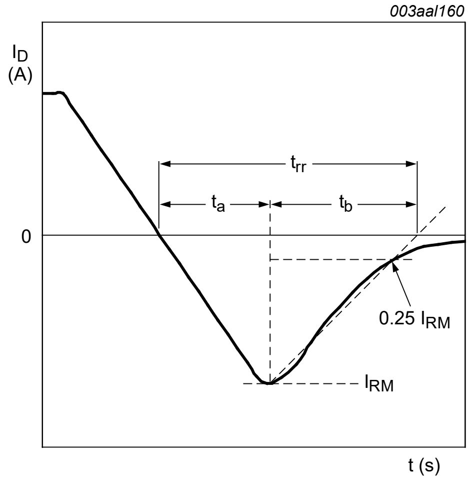
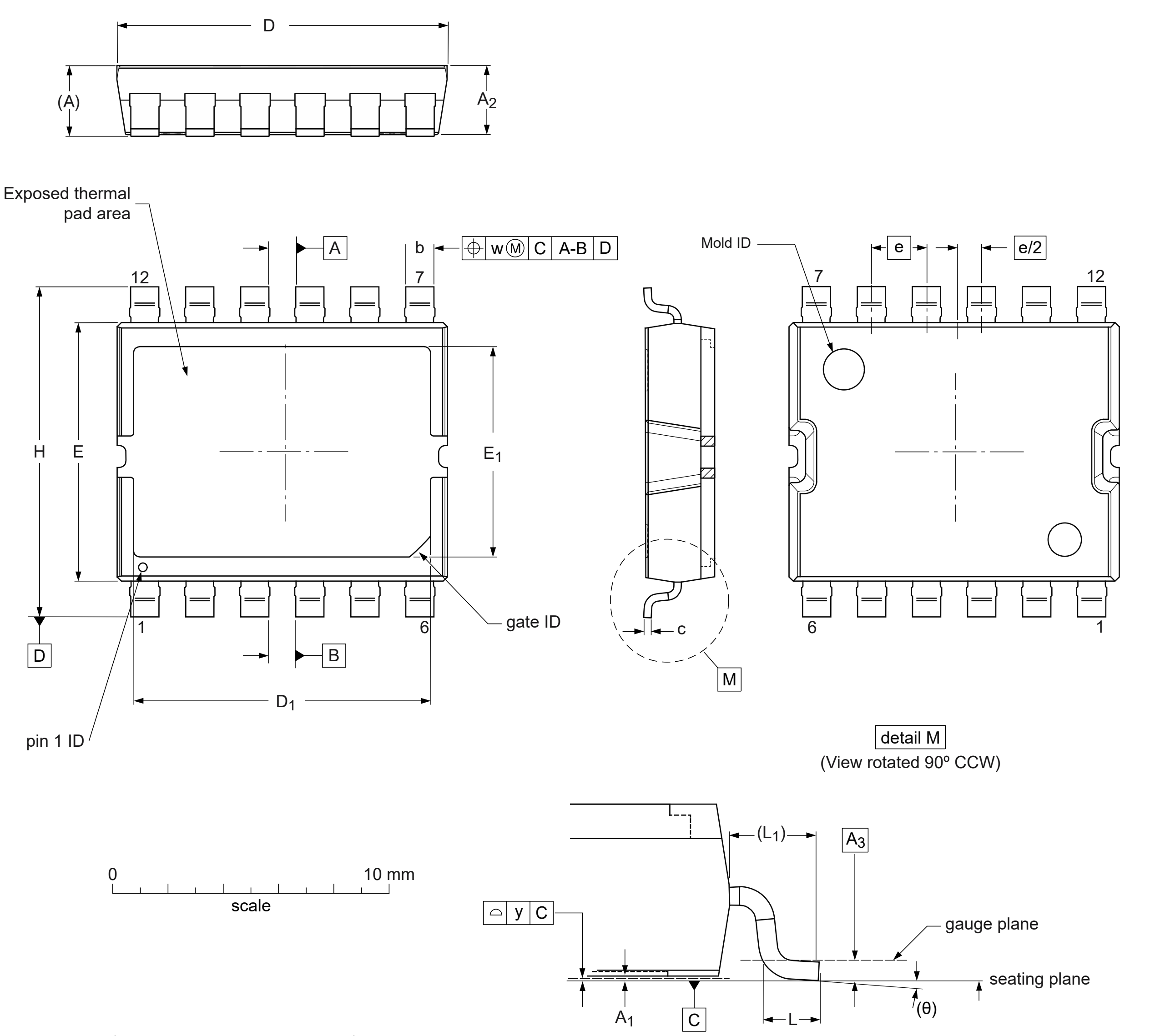


Fig. 15. Reverse recovery timing definition

11. Package outline

SOT8005A: Plastic, surface mounted copper clip package (CCPAK1212i); 12 terminals; 2.0 mm pitch, 12 mm × 12 mm × 2.5 mm body **SOT8005A**



Dimensions (mm are the original dimensions)

Unit[1]		A(ref)	A_1	A_2	$\boxed{A_3}$	b	c	D	D_1	E	E_1	$\boxed{e}$	H	L	L_1(ref)	w	y	θ(ref)
mm	max		0.13	2.525		1.12	0.30	12.15	10.95	9.55	7.40		12.15	1				
	nom	2.63			0.25							2.0			1.3	0.20	0.1	4°
	min		0	2.475		0.93	0.22	11.85	10.65	9.25	7.10		11.85	0.6				

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included for dimension D.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included for dimension E.

sot8005a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8005A		MO-359				~~25-04-14~~ 25-05-06

Fig. 16. Package outline CCPAK1212i (SOT8005A)

12. Soldering

Footprint information for reflow soldering of CCPAK1212i package **SOT8005A**

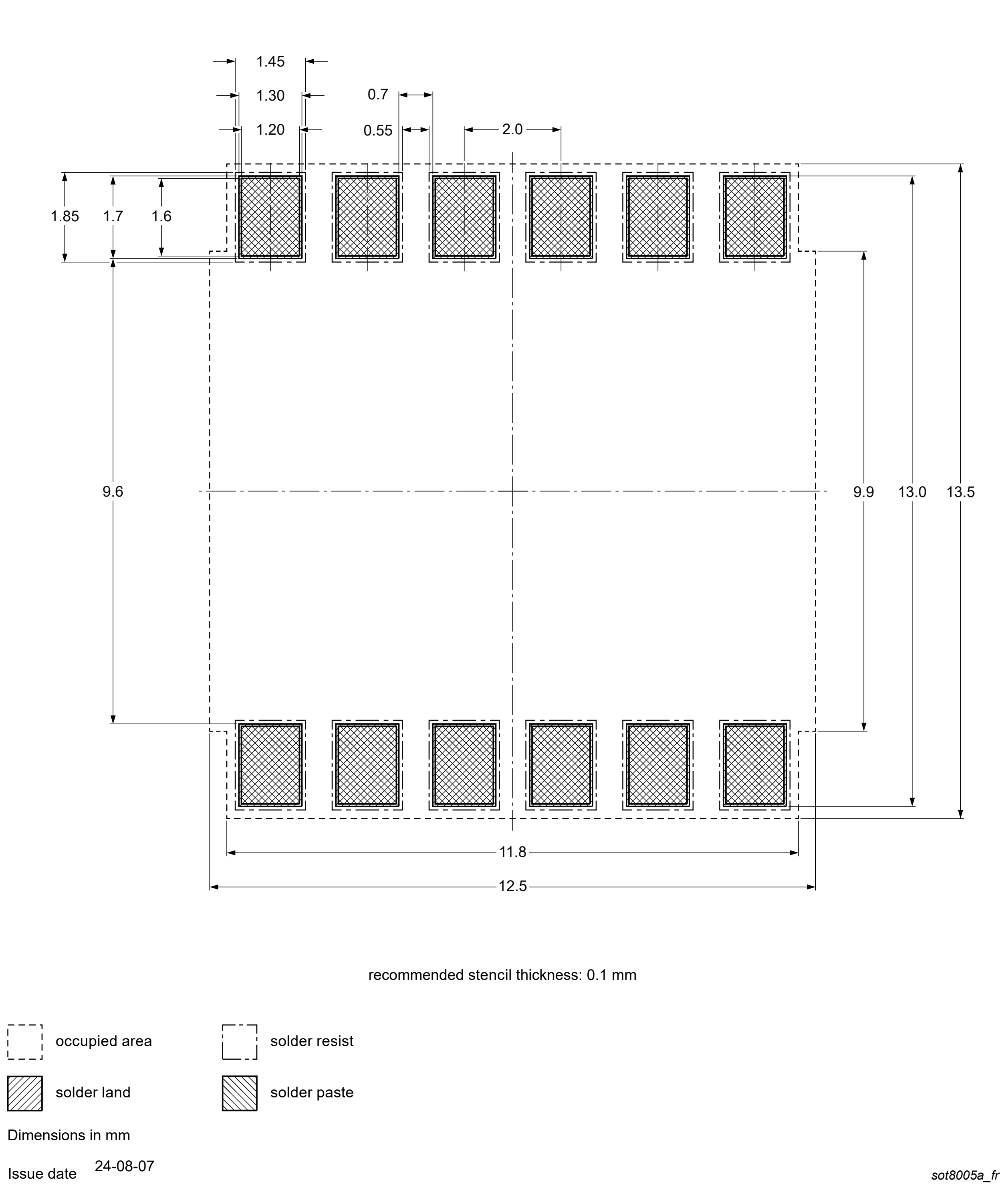


Fig. 17. Reflow soldering footprint for CCPAK1212i (SOT8005A)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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Date of release: 26 August 2025